Near Optimal Automatic Chip Design

Licence Opportunity

Electronic Design Automation (EDA) research at Oxford Brookes University, led by Dr. Abusaleh Jabir, has culminated in a novel synthesis technique, called GfXpress™, for the automatic synthesis and optimization of multivariate, multiple output polynomials over finite fields. Industrial partners are sought for further development and to bring this innovative technology to market.

This technique has many practical applications, but is particularly applicable for the design of cryptographic hardware, e.g. the elliptic curve cryptosystems, parts of the AES system, error control and correction schemes (e.g. the BCH and Reed-Solomon coders), digital signal processors, etc.

As the market continues to demand smaller more mobile systems, which run on batteries, the need to use less power becomes a key driver and competitive imperative. Laboratory experiments have shown that, GfXpress™ can demonstrate an order of magnitude improvement, with respect to power, speed and area, over current state of the art systems. In this industry, an improvement of 20% is regarded as significant; the GfXpress™ research prototype has demonstrated up to 68 times improvement! This can provide adopters with a significant competitive advantage.

Current techniques all involve a hand-coding stage. With GfXpress™ the process is completed automatically. This can provide designers and their clients with huge cost benefits.

With GfXpress™ verifiable hardware is produced. Unlike all other techniques GfXpress™ produce optimal or near optimal designs, which are "canonic", i.e. the exact same and structurally identical result (circuit) for systems with the same functionality, which is independent of the initial starting point. This provides the additional extremely valuable benefit of producing “verifiable” hardware, which is not possible with most existing systems. This will give designers and their clients cost benefits, performance, and design confidence.

GfXpress™ is capable of producing 100% testable circuits against manufacturing faults. These faults can result from imperfections in the silicon wafers, inadvertent solder splashes, etc. and cause the circuits to malfunction at the end user stages, unless they are tested once they have gone through the production lines. The number of test vectors required, which is the measure of the testing time, for testing the synthesized circuits against these faults is very small. This is an extremely important feature of the tool, since all the industrial designs must be tested against these manufacturing faults. Making circuits testable again against these faults is known to be a very hard problem, which the proposed technique incorporates by default very efficiently. This has been verified with the help of the premier industrial tools.

- GfXpress™ produces a near optimal circuit layout automatically, unlike many current systems, which include a manual stage.
- Laboratory prototype demonstrates orders of magnitude improvements in area, power and speed compared to current solutions.
- The final circuits are independent of initial specs, allowing the hardware designs to be easily verifiable with enhanced testability. Most existing tools cannot produce easily verifiable hardware.
The techniques in GfXpress™ are protected by an international patent application. Searches show both novelty and inventiveness.

The techniques and approach has been validated by industry experts and published in several peer reviewed premier journals and conferences. These include:

- Proc. IEEE/ACM International Conf. on Computer Aided Design (ICCAD), Silicon Valley, USA, Nov. 2006

Dr. Abusaleh Jabir is an IEE Hartree Premium Award winner. He delivered the Distinguished Keynote Speech at the International Conference on Computing and Information Technology, (2005). For a full list of publications please contact us.

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